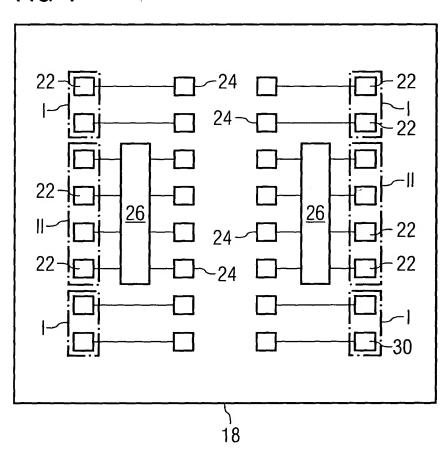
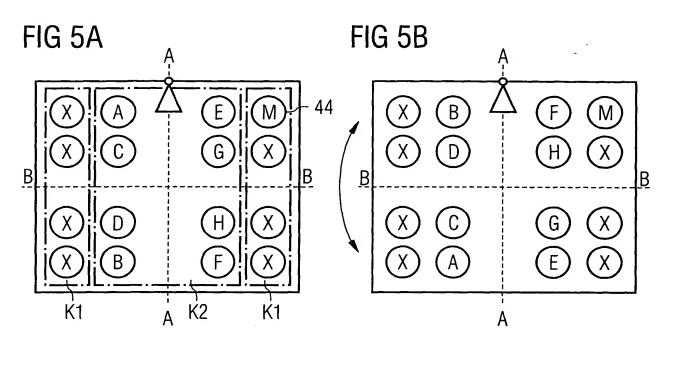


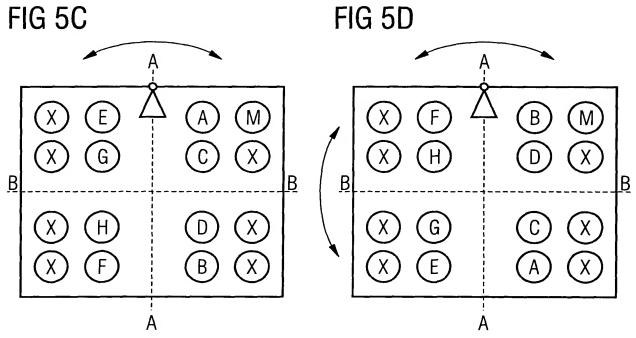
FIG 4



SEMICONDUCTOR MEMORY APPARATUS WITH VARIABLE CONTACT CONNECTIONS, AND A CORRESPONDING

SEMICONDUCTOR APPARATUS





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Applicant(s): Andreas Tauber
SEMICONDUCTOR MEMORY APPARATUS WITH VARIABLE
CONTACT CONNECTIONS, AND A CORRESPONDING
SEMICONDUCTOR APPARATUS

FIG 6

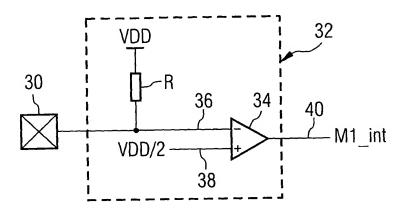
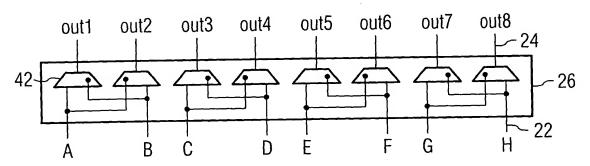


FIG 7A



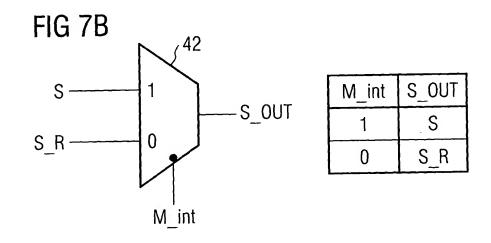
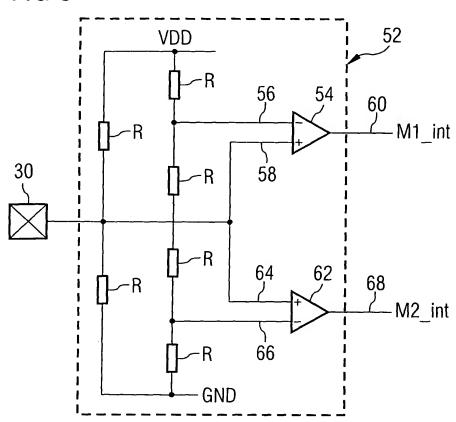


FIG 8



M1_int M2_int

M1_int	M2_int	S_OUT	
0	1	S	
1	1	S_R	
0	0	S_Rr	

FIG 10

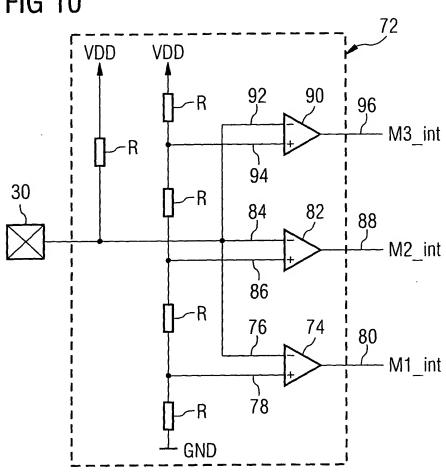
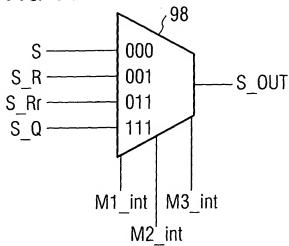


FIG 11



M1_int	M2_int	M3_int	S_OUT
0	0	0	S
0	0	1	S_R
0	1	1	S_Rr
1	1	1	S_Q